Amdt. Dated June 13, 2005

Reply to Office action of March 16, 2005

## **Specification:**

Add new paragraphs [0020.1], [0020.2], [0058.1], and [0058.2] as follows:

[0020.1] FIG. 10 shows a MISHFET gas sensor device in accordance with an embodiment of the invention.

[0020.2] FIG. 11 shows a MISFET gas sensor device in accordance with an embodiment of the invention.

[0058.1] FIG. 10 illustrates MISHFET a gas sensor device 48' in accordance with an embodiment of the invention. The gas sensor device 48' is similar in structure to the gas sensor device 48 (FIG. 4), except in the make-up of the catalytic gate-electrode. Specifically, the catalytic gate-electrode 58 illustrated in FIG. 10 includes a layer 58' of a metal oxide. The layer 58' serves as both a catalytic component and as an insulating component. The metal oxide making up the layer 58' may include any metal oxide suitable for serving as both a catalyst and an insulator, including those selected from the group consisting of gallium oxide, silver oxide, indium oxide, vanadium oxide, Mn<sub>2</sub>O<sub>3</sub>, CuO, Cr<sub>2</sub>O<sub>3</sub>, Co<sub>2</sub>O<sub>3</sub>, ZnO, Ge<sub>2</sub>O<sub>3</sub>, FeO<sub>2</sub>, bismuth molybdates, and any combinations thereof. The combination of the catalytic gate-electrode 58, including the combined catalytic and insulating portion 58', and the heterostructure barrier layer 52 within the semiconductor substrate 50 forms a metal insulator semiconductor heterojunction field effect transistor (MISHFET).

[0058.2] FIG. 11 illustrates a gas sensor device 62' in accordance with an embodiment of the invention. The gas sensor device 62' is similar in structure to the gas sensor device 62 (FIG. 5), except in the make-up of the catalytic gate-electrode. Specifically, the catalytic gate-electrode 70 illustrated in FIG. 10 includes a layer 70' of a metal oxide. The layer 70' serves as both a catalytic component and as an insulating component. The metal oxide making up the layer 70' may include any metal oxide suitable for serving as both a catalyst and an insulator, including those selected from the group consisting of gallium oxide, silver oxide, indium oxide, vanadium oxide, Mn<sub>2</sub>O<sub>3</sub>, CuO, Cr<sub>2</sub>O<sub>3</sub>, Co<sub>2</sub>O<sub>3</sub>, ZnO, Ge<sub>2</sub>O<sub>3</sub>, FeO<sub>2</sub>, bismuth molybdates, and any combinations thereof. The combination of the catalytic gate-electrode 70, including the combined catalytic and insulating

portion 70', and the semiconductor substrate 64 forms a metal insulator semiconductor field effect transistor (MISFET). The presence of metal oxide within the layer 70' also allows the gas sensor device 62' to be considered a metal oxide semiconductor field effect transistor (MOSFET).

Amend paragraph [0055] as follows:

[0055] FIG. 6 shows still yet another example of a gas sensor device in a MOSFET configuration. In this example of a MOSFET configured gas sensor device, a silicon carbide n-type substrate 76 has thereon a P-epitaxial layer 78, such as 5el5 p-type epitaxial layer of 4 micrometers (µm) thickness. A mesa 80 is etched by depositing a resist, imaging, patterning, etching the epitaxial layer 56, and stripping the resist. An n-channel 92 is implanted by depositing and densifying 1 μm HTO oxide layers, using photoresist mask and RIE etch oxide, depositing screen oxide, implanting in the epitaxial layer 78 an n-channel 82 using 3 implants to get a box profile at 600° C, 180 KeV, n ions, and stripping the oxide. An N+ source 84 and an N+ drain 86 are implanted by depositing and densifying 1 µm HTO oxide layers, using photoresist mask and RIE etch oxide, depositing screen oxide, implanting in the epitaxial layer 78 an N+ source 84 and an N+ drain [84] 86 using 3 implants to get a box profile at 600° C, n ions, and stripping the oxide. A P+ implant 88 for top or body contact is ion implanted by depositing and densifying 1 µm HTO oxide layers, using photoresist mask and RIE etch oxide, depositing screen oxide, implanting in the epitaxial layer 78 a P+ contact 88 using 4 implants to get a box profile at 1000° C, 180 KeV, Al and/or C ions, and stripping the oxide. The implants 82, 84, 86, and 88 are then annealed at 1,300° C. Sacrificial oxidation may be required for removing surface damage. A field oxide layer 90, such as  $SiO_2$ , is grown by thermal oxidation at 300 Angstroms, depositing and densifying 1 µm HTO oxide and phosphorous silicate glass (PSG), photoresist patterning, ICP etch (80%), and wet etch (20%) in channel. The field oxide 90 helps to protect the surface of the gas sensor device. A gate oxide 92, such as a high quality SiO<sub>2</sub>, is grown by 1,100° C steam oxidation (500 Angstroms), 950° C steam re-oxidation anneal. A gate metal 94, such as nickel or molybdenum, is deposited by photopatterning, evaporating or sputtering about 4000 Angstroms of gate metal, and removing photoresist. Ohmic contacts [94 and 96], such as nickel and/or gold, are deposited using photopatterning with oxide etchback, evaporating or sputtering the nickel and/or gold, and liftoff of metal. A P-ohmic [98], such as Ti/Al and/or Ni/Al is deposited using photopatteming with oxide etchback, evaporating/sputtering Ti/Al and/or Ni/Al layers on top of P+ contact 88, lifting off metal, annealing ohmics [94, 96 and 98] at 975° C (N<sub>2</sub> and/or Ar atmosphere for about 2 minutes). Gate metal 94 is deposited by photopatterning, evaporating/sputtering 300 Angstroms of catalytic gate electrode material, stripping photoresist, and annealing at 600° C to activate catalyst. Overlay 100, such as Ti/Ni/Au is deposited using photopatteming, evaporating Ti/Ni/Au, and stripping the photoresist. A passivation layer 102 is deposited. It should also be noted that although this example shows a single catalytic gate electrode, one or more catalytic gate electrodes may be part of each gas sensor device and/or an array of gas sensor devices may be employed.